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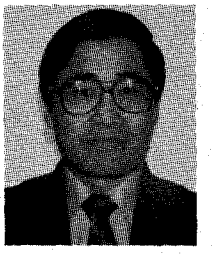
In 1974 she joined the Corporate Research and Development Center of the General Electric Company. Her research in that laboratory centered on beam (ion, electron, and laser) effects in semiconductors studied through a variety of analytical techniques, especially electron microscopy (EBIC). The development of beam-addressed memory devices utilized the findings of these studies. She holds five patents in this area. Her work at General Electric also entailed other applications of beams for imaging and display devices, electron lithography and microscopy, ion implantation, and laser and electron beam annealing. In 1979 she joined Rockwell Science Center, where her work has included the study of ion implantation effects in GaAs, and the investigation of beam annealing and alloying in GaAs. She presently directs the activities of members of the Materials Technology Section, whose efforts are centered on ion implantation, encapsulation, bulk growth, and characterization of GaAs. She has authored or coauthored more than 30 publications in the areas of ion and electron beam effects and semiconductor materials.

Dr. Kirkpatrick is a senior member of the Society of Women Engineers, and a member of the American Physical Society.



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Proton Isolation for GaAs Integrated Circuits

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Abstract—**Significant improvement in the electrical isolation of closely spaced GaAs integrated circuit (IC) devices has been achieved with proton implantation. Isolation voltages have been increased by a factor of four in comparison to a selective implant process. In addition, the tendency of negatively biased ohmic contacts to reduce the current flow in neighboring MESFET's (backgating) has been reduced by at least a factor of three. The GaAs IC compatible process includes implantation of protons through the SiO_2 field oxide and a three-layered dielectric–Au mask which is definable to 3-μm linewidths and is easily removed. High temperature storage tests have demonstrated that proton isolation, with lifetimes on the order of 10^5 h at 290°C, is not a lifetime limiting component in a GaAs IC process.**

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I. INTRODUCTION

THE SUCCESSFUL design and fabrication of medium- and large-scale GaAs integrated circuits (IC's) requires a high degree of electrical isolation between closely spaced active devices. Traditionally, mesa etched [1], [2] and selective implant [3] processes have been used to isolate GaAs IC's. These processes can result in significant current flow

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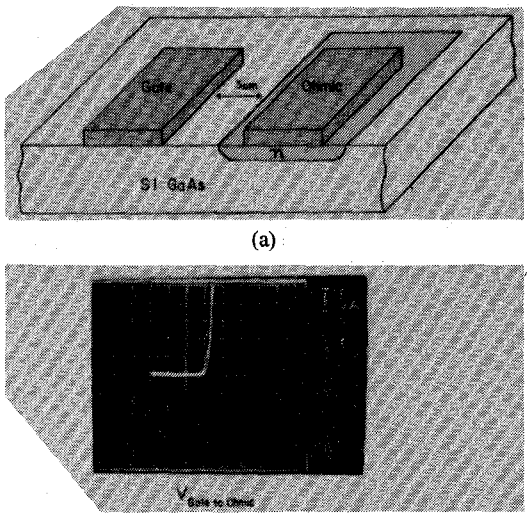

(a)

(b)

Fig. 1. (a) Cross section of a gate-to-ohmic isolation test pattern fabricated with a selective implant process. (b) Curve-tracer photograph of the current–voltage characteristic for the test pattern diagrammed in (a).

between isolated patterns separated by five microns or less. In this work, proton implantation is used to achieve a dramatic improvement in the electrical isolation of GaAs IC's.

A typical isolation characteristic for a selective implant process is displayed in Fig. 1. The test pattern consists of a gate metallization on semi-insulating GaAs separated by 3 μm from an ohmic-contacted n-type region. The measured current versus voltage characteristic is rectifying. Significant current flows when the gate metal is biased positively with respect to the ohmic contact, but negligible current flows with the reverse polarity. While the 5.0-V breakdown or isolation voltage is typical for selective implant and mesa isolated structures, lower isolation voltages, on the order of 2.0 V, are often observed. The variability in isolation voltage can be partially attributed to surface conditions, including chemical treatments and the presence or absence of dielectric passivation. Asymmetric characteristics are also observed when an ohmic metallization directly contacts the semi-insulating GaAs substrate. In both cases, high fields at the edges of the metal/semi-insulating GaAs interfaces are believed to be responsible for the relatively low breakdown voltages.

A second detrimental effect related to insufficient isolation is backgating. It occurs when a negatively-biased n-type region is in close proximity to an operating GaAs MESFET. As the negative bias on the ohmic contact is increased, the active layer-substrate depletion region beneath the MESFET widens, resulting in decreased current flow. In a typical mesa or selective implant wafer the drain current is reduced by 10 percent with only -3.0 V applied to a backgating ohmic contact separated from the MESFET by 5.0 μm.

The relatively low degree of electrical isolation in mesa and selective implant processes can lead to significant circuit design constraints, including an increase in minimum spacing rules, reduction in packing density, and severe design complications. Proton implantation constitutes a potentially superior isolation process. Implantation of protons into GaAs has been used successfully to isolate discrete diodes, lasers, and MESFET's [4]–[11]. Extensive characterization has indicated that proton damage is capable of producing high resistivity, thermally stable layers in both n and p type GaAs [4]–[9]. Recently proton [12], [13], as well as boron [14] and oxygen [15], ion-implantations have been applied to linear and digital monolithic IC's.

This paper describes a GaAs IC-compatible proton isolation process, with emphasis on the electrical (isolation and backgating) characteristics important to medium- and large-scale integration. Proton damage characterization and process development are presented in the second section. Measurement results including isolation, backgating, and reliability are described in the third section. The fourth section contains a summary of the work and important conclusions.

II. Process Development

The major objective in developing an IC-compatible proton isolation process is to eliminate isolation as a design consideration. The HP Santa Rosa GaAs IC process [16] is designed to fabricate small- and medium-scale gigahertz-bandwidth digital and analog IC's. For this type of technology, greater than 10-V isolation is required between patterns separated by the minimum spacing of 3.0 μm. To achieve this goal, a proton implantation mask must be designed which can be defined to a width of 3.0 μm while adequately protecting active areas from proton damage. In addition, the protons must be implanted through the SiO_2 anneal cap which is retained as a field oxide in order to optimize surface passivation and minimize process complexity [16]. The process features to be established are: the minimum implant energy required to achieve sufficient isolation; and the optimum dose for the specific active layer profile and temperature processing [16].

A. Proton Damage Characterization

Proton implantation into GaAs creates damage centers which effectively trap electrons and holes. These traps reduce the conductivity of an active layer by removing mobile electrons from the conduction band.

The damage profile has been characterized by measuring the mobile carrier concentration (with the CV technique) before and after partially compensating proton implantations. These measurements have been performed over a range of implant energies and doses. Typical results are plotted in Fig. 2. The initial electron profile is constant at 6×10^{16} cm^{-3} to a depth of 0.6 μm. Protons are implanted through the 4200-Å SiO_2 field oxide at an energy of 110 keV, which is large enough to penetrate the active layer. The electron profile is remeasured indicating the shape and magnitude of the as-implanted proton damage as a function of proton dose and energy. The results in Fig. 2

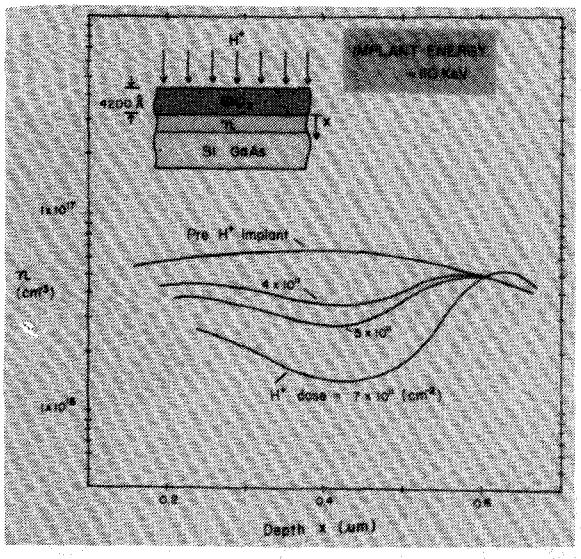

Fig. 2. The electron concentration n versus depth (measured by the CV technique) before and after partially compensating proton implantations. The protons are implanted through 4200 Å of SiO_2.

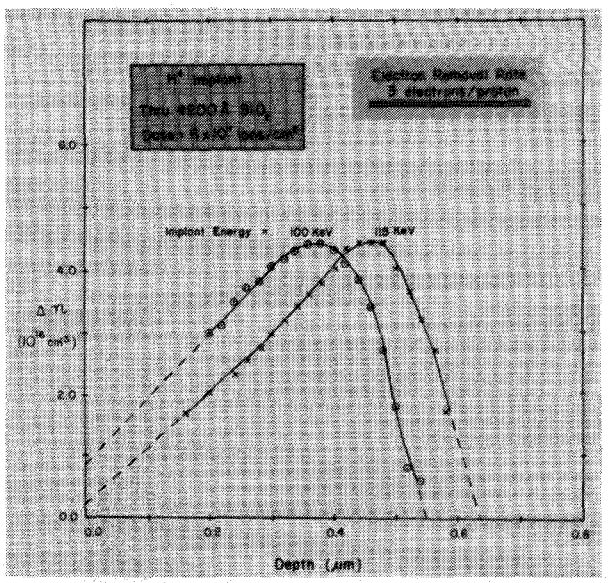

Fig. 3. Electron removal Δn versus depth for two implantation energies.

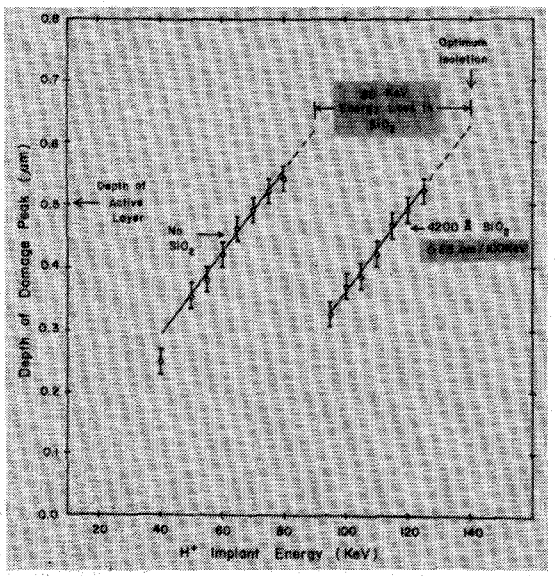

Fig. 4. Depth of as-implanted proton damage peak versus implantation energy with and without 4200-Å SiO_2 field oxide.

indicate that the damage (electron removal) concentration increases linearly with dose for the relatively low, partially compensating proton doses shown (4.0, 5.0, and 7.0×10^{11} cm^{-2}).

The concentration of electrons trapped or removed from conduction, Δn, can be computed as a function of depth by subtracting the electron profile after proton implantation from the initial electron profile. The results for a dose of 6.0×10^{11} protons/cm^{-2} and energies of 100 and 115 keV are plotted in Fig. 3. The protons are implanted through the field oxide. The total number of electrons removed from conduction can be estimated by integrating the electron removal profiles. Dividing the integral by the proton dose results in an electron removal rate of three electrons per proton. This implies that, at this relatively low dose, the average proton creates enough damage to trap three electrons. As will be discussed below, the electron removal rate may be somewhat lower for the high proton doses required for complete compensation.

The electron removal characteristics plotted in Fig. 3 indicate that the shape of the damage profile is relatively independent of implantation energy while the depth of the as-implanted damage profile increases with increasing energy. This effect is examined more closely in Fig. 4 where the depth of the damage peak is plotted as a function of energy for proton implantations with and without the SiO_2 field oxide. In both cases, the depth of the damage peak increases at a rate of 0.65 μm/100 keV. The offset between the damage peaks with and without the anneal cap indicates that protons lose approximately 50 keV in passing through the 4200-Å SiO_2 field oxide.

Current–voltage measurements demonstrate that the minimum energy required to achieve optimum isolation for the GaAs IC active layer profile [16] is 140 keV. Extrapolating the data in Fig. 4 implies that the depth of the damage peak is located at 0.62 μm for proton implantation through 4200 Å of SiO_2 at 140 keV. For the high doses required for complete compensation (between 1.0×10^{14} and 1.0×10^{15} protons/cm^2), significant damage extends beyond the depth of the damage peak. After proton implantation through the field oxide, with a dose of 5×10^{14} protons/cm^2 and energy of 140 keV, CV measurements indicate full compensation extends to approximately 0.9 μm. Since the 140-keV implant through the oxide corresponds to a 90-keV implant directly into GaAs, the measured depth agrees well with previously reported values [4], [8] between 0.85 and 1.0 μm/100 keV. The total damage depth is a factor of two larger than the depth of the GaAs IC active layer profile. For the same implantation conditions, the lateral spread of protons from a mask edge has been estimated (from measurements on narrow resistors) to be between 0.6 and 0.7 μm. This is consistent with experimental and theoretical values reported in the literature [7], [17].

The second implantation parameter to be considered is

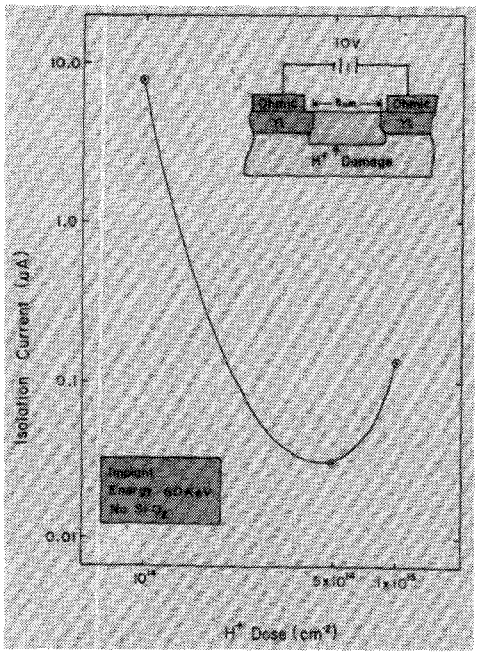

Fig. 5. Isolation current versus proton dose for two ohmic contacts separated by 5.0 μm of proton damaged area with 10 V applied.

the proton dose. To determine the dose required to achieve sufficient isolation the current–voltage characteristics have been measured between two ohmic contacts separated by 5.0 μm of proton damaged area. The initial active layer is formed by a Si implantation and has a peak concentration of 2.0×10^{17} cm^{-3} at a depth of 0.2 μm [16]. The isolation current with 10 V applied is plotted as a function of dose in Fig. 5. While sufficient isolation is achieved between 1.0×10^{14} and 1.0×10^{15} protons/cm^2, the minimum isolation current (for the three doses included in this experiment) occurs at 5.0×10^{14} protons/cm^2. The increase in isolation current with increasing dose has been previously reported [6] and may be caused by defect-level banding [6] or enhanced hopping conduction mechanisms [9]. While the data presented in Fig. 5 are for unbaked samples with 60-keV proton implantations directly in GaAs, similar results are observed for 140-keV implantations through the SiO_2 field oxide, both before and after a four hour 300°C bake included in the GaAs IC process [16].

The apparent optimum dose is two orders of magnitude greater than what would be predicted from the low dose electron removal rate (Fig. 3). Several factors may contribute to the discrepancy. First, excess damage beyond that needed to trap all the conduction electrons can reduce the mean free path and as a result the electron mobility. Secondly, the maximum depth of damage increases with increasing dose, so that a larger portion of the substrate is converted to very high resistivity material. Finally, electron removal may not increase linearly with dose at high dose levels.

The optimum proton implantation parameters are established at 140 keV and 5.0×10^{14} cm^{-2}. The final process consideration is the development of a proton mask.

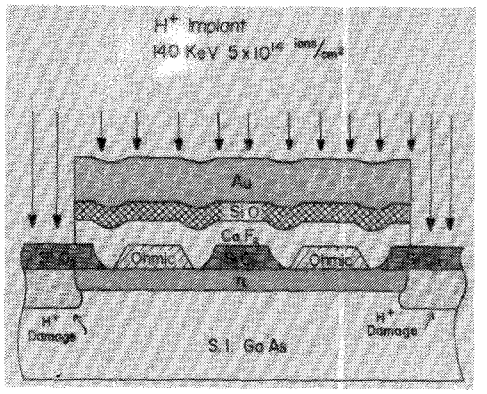

Fig. 6. Schematic cross section of a GaAs IC at the proton isolation step.

B. Proton Implantation Mask

The proton implantation mask must meet three requirements to be compatible with the GaAs IC process. First, it must stop protons implanted at 140 keV in order to effectively protect active areas. Second, the mask must be definable to the minimum linewidth of the IC process, 3.0 μm in this case. Finally, the mask must be easily removable with a process that is nondamaging to the exposed GaAs surface. Those objectives were achieved with a three-layer mask composed of CaF_2, SiO, and Au defined by a photoresist lift. Before describing the details of this process it will be helpful to briefly review the preceding fabrication steps [16].

The first step in the GaAs IC process is a direct, unmasked implantation of Si (6.25×10^{12} cm^{-2}, 230 keV) into high purity or lightly Cr-doped (less than 1.0×10^{15} cm^{-3}) substrates. This active layer implant is annealed after capping with 4200 Å of low temperature, CVD, SiO_2. The anneal cap is retained in field areas during subsequent processing. In the next step, ohmic contacts are deposited and alloyed.

The proton isolation mask, composed of the two dielectric layers and 1.3 μm of Au, is defined by a positive photoresist lift. A schematic cross section of the final structure is displayed in Fig. 6. Protons are then implanted at 140 keV to a dose of 5.0×10^{14} cm^{-2}. In the field areas, protons penetrate the SiO_2 and enter the GaAs with an effective approximate energy of 90 keV. The resulting damage creates a high resistivity layer to a depth of 0.9 μm. The Au–dielectric mask protects the active areas during the proton implantation. Finally, the mask is readily removed by etching the CaF_2 in dilute HCl. To date, this masking scheme has been used successfully in 20 production-prototype runs including over 100 wafers. The following sections present electrical measurement results for the proton isolation process.

III. Results

A. Isolation

The gate-to-ohmic isolation characteristics, typical of the selective implant and the proton implant processes, are

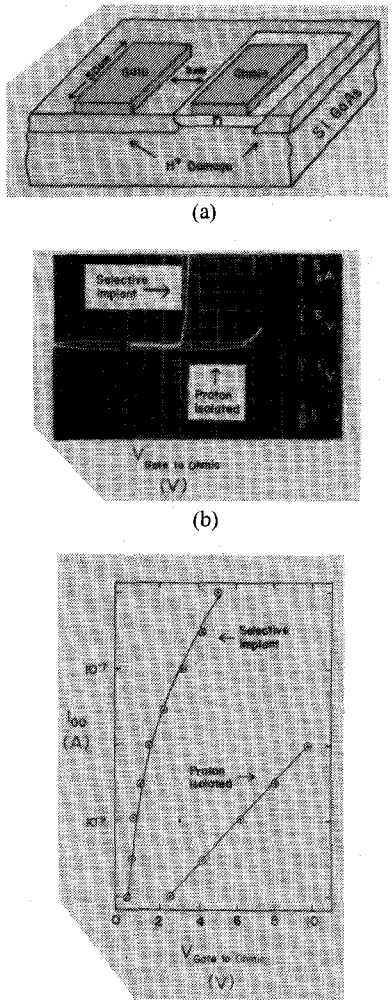

Fig. 7. (a) Cross section of a gate-to-ohmic isolation test pattern fabricated with a proton implantation process. (b) Curve-tracer photograph comparing the gate-to-ohmic isolation characteristics for typical selective implant and proton isolated processes. (c) Gate-to-ohmic isolation current I_{GO} versus voltage for typical selective implant and proton isolation processes.

compared in Fig. 7. The test pattern consists of a 50-μm-long gate metallization directly on high resistivity, proton implanted, GaAs separated by 3.0 μm from an ohmic-contacted n-type region. Both measurements are on fully processed wafers including a four hour bake at 300°C. The curve tracer photograph indicates that no significant current flows in the forward direction below 20 V for the proton isolated process. This value of isolation voltage is a factor of four greater than the value obtained with the selective implant process. Significant improvement is also realized at low current levels, as is demonstrated in Fig. 7(c). At typical IC operating voltages the isolation current is three orders of magnitude less for the proton isolated pattern. Even for a worst case IC operating voltage of 10 V, only 10 nA of isolation current flows for the proton isolated process.

A second test pattern is used to evaluate ohmic-to-ohmic isolation. It consists of two 50-μm-long ohmic-contacted n-type regions separated by a 3-μm-wide high resistivity

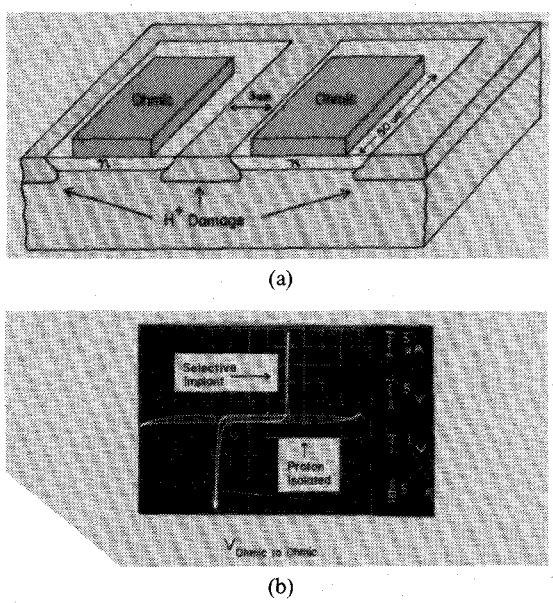

Fig. 8. (a) Cross section of an ohmic-to-ohmic isolation test pattern fabricated with a proton implantation process. (b) Curve-tracer photograph comparing typical ohmic-to-ohmic isolation characteristics for proton implant and selective implant processes.

proton implanted region, as shown in Fig. 8(a). For this test pattern the isolation characteristics, displayed in Fig. 8(b), are symmetric. Again, considerable improvement is obtained with proton isolation, in which case no significant current flows below 25 V. In contrast, large values of isolation current are observed at approximately 10 V for the selective implant process.

The preceding results indicate that significant improvement can be obtained with a proton isolation process. In fact, the results demonstrate that proton implantation eliminates isolation as a design constraint. The next section compares backgating effects for the two processes.

B. Backgatiang

Backgating occurs in a GaAs IC when a negatively biased ohmic-contacted n-type region is in close proximity to an operating MESFET. As the negative bias increases, the depletion region at the interface between the MESFET and the semi-insulating substrate widens, resulting in a reduction in drain current. Backgating is an extremely undesirable effect in an IC. When significant backgating occurs, FET dc characteristics depend not only on the internal device biases but also on the proximity of negative voltage lines. Normally straightforward design considerations, such as dc operating points and matching between devices, become layout dependent, leading to severe design complications and a relaxation of minimum design rules. The following results demonstrate that proton isolation helps avoid these problems by significantly reducing the susceptibility of GaAs IC's to the backgating effect.

The test pattern used to characterize backgating is schematically drawn in Fig. 9. The structure consists of a 100-μm-wide MESFET and a negatively biased, backgating, ohmic contact. To maximize backgating sensitivity, the

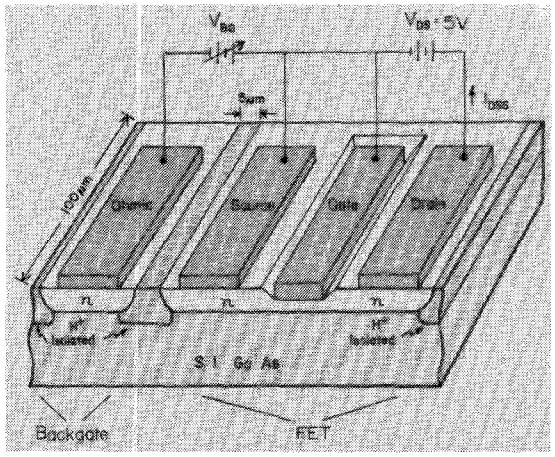

Fig. 9. Schematic cross section of the GaAs IC backgating test pattern.

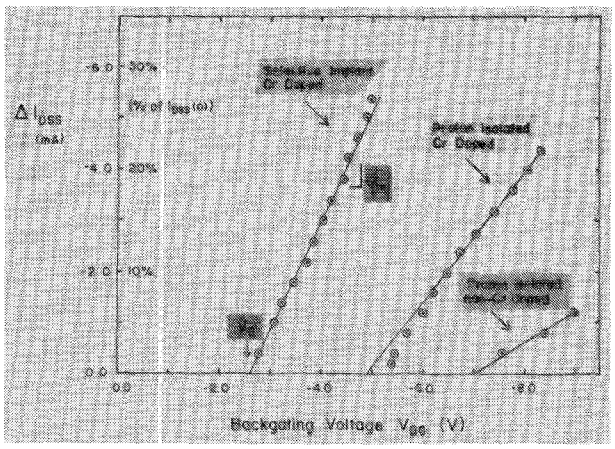

Fig. 10. Change in drain current ΔI_{DSS} versus backgating voltage V_{BG} measured on the test pattern diagrammed in Fig. 9. Typical characteristics for three groups are plotted: selective implant on lightly Cr-doped substrates, proton isolated on lightly Cr-doped, and proton isolated on non-Cr-doped.

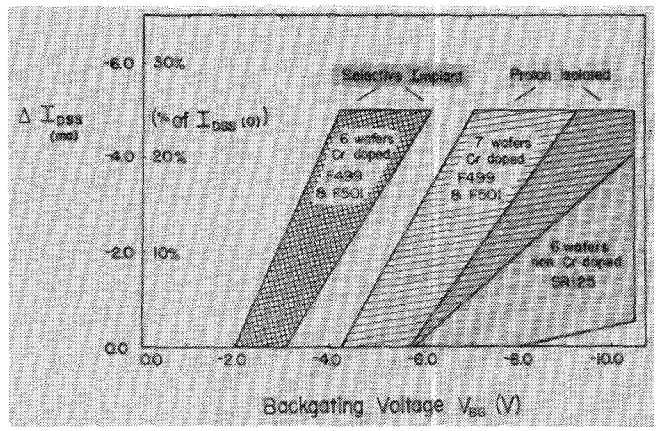

Fig. 11. Distribution in wafer averages of backgating threshold and transconductance for three groups of wafers: selective implant on lightly Cr-doped substrates, proton isolated on lightly Cr-doped, and proton isolated on non-Cr-doped. F499, F501, and SR125 are ingot identification numbers.

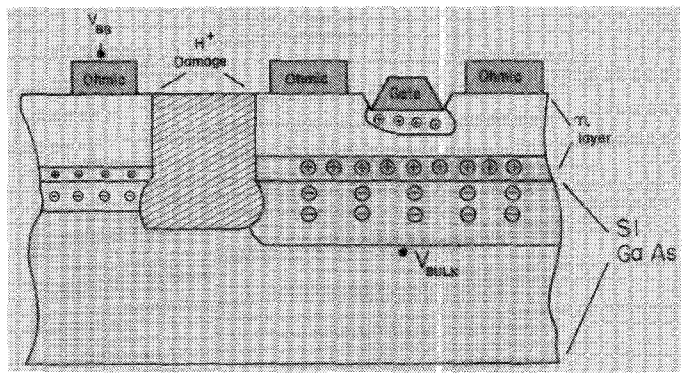

Fig. 12. Cross section of a GaAs MESFET in close proximity to a backgating ohmic contact.

ohmic-contacted n-type region runs the full width of the MESFET and is separated by 5.0 μm from the source. The MESFET is operated at $V_{DS} = 5.0$ V and $V_{GS} = 0.0$ V. For these bias conditions, the drain current and transconductance are nominally 20 mA and 12 mS, respectively [16]. Backgating is characterized by measuring the change in drain current ΔI_{DSS} as a function of backgating voltage V_{BG}.

Typical backgating characteristics for three groups of fully processed wafers (including a four hour bake at 300°C) are plotted in Fig. 10. In all cases, the change in drain current increases linearly with negatively increasing backgating voltage. The characteristics are well defined by a backgating threshold V_T below which no significant backgating occurs, and a backgating transconductance G_m equal to the slope of the line. For the selective implant process on lightly Cr-doped (less than 1.0×10^{15} cm^{-3}) substrates the threshold is approximately -2.5 V. At a typical IC operating voltage of -5.0 V, the current has decreased by an intolerable 30 percent. In contrast, with proton isolation on lightly Cr-doped material, no significant backgating occurs below 5.0 V. In addition, the backgating transconductance is halved. At a worst case IC operating voltage of -6.0 V, less than 10-percent reduction in drain current is observed. Further improvement is obtained with proton isolation on non-Cr-doped substrates. In this case, the backgating threshold is extended beyond the range of normal circuit operation to -7.0 V.

The backgating threshold and transconductance have been characterized on a large number of completed wafers. One hundred percent of the test patterns are measured and wafer averages are computed for both parameters. The spread in wafer averages for the three groups are graphically displayed in Fig. 11. For the selective implant process on lightly Cr-doped substrates, the threshold can be as low as -2.0 V, resulting in a 25-percent decrease in drain current at only -4.0 V. In contrast, the minimum thresholds observed for proton isolated wafers on lightly Cr-doped and on non-Cr-doped substrates are approximately -4.0 and -6.0 V, respectively.

The preceding results demonstrate that proton isolation significantly decreases the susceptibility of GaAs IC's to the backgating effect. The improvement is gained by proton implantation's ability to increase the resistivity of GaAs in the field area, between the backgating pad and the active MESFET. The structure is schematically diagrammed in Fig. 12. According to current understanding of backgating [18]–[20], the degradation in drain current

results from the spread of the back depletion region into the active layer of the FET. The width of the interfacial depletion region primarily depends on two factors. The first is the concentration of defects and impurities which can trap electrons or emit holes creating fixed negative charge in the substrate. The second factor is the voltage developed across the depletion region. Proton implantation does not affect the concentration of traps beneath the FET. Instead, proton damage reduces the voltage developed across the interfacial depletion region in response to the applied backgating voltage, by increasing the resistivity of the field region between the MESFET and the backgating pad.

It has been observed that both isolation and backgating for the selective implant process are sensitive to surface conditions, including chemical treatment and dielectric passivation. The fact that mesa isolation is comparable to selective implant in isolation and backgating characteristics also implies that the surface plays a significant role. One of the prime advantages of proton isolation is that the high dose implantation creates a fairly uniform damage layer from the surface to a depth of approximately 1 μm. In this way, proton implantation not only compensates the active layer, but also passivates the surface. As a result, proton-isolated IC's are relatively insensitive to surface conditions. In the next section, thermal stability of proton damage is investigated.

C. Thermal Stability

Proton implantation compensates an active layer by creating lattice defects which trap mobile electrons and holes. It can be expected that the lattice damage will anneal out at a sufficiently high temperature. Previous work has demonstrated that high-resistivity proton-implanted layers are maintained for relatively short anneal times up to temperatures of 400°C for single implantations [4], [8] and 500°C for multiple implantations [7], [9], [21]. However, specific annealing characteristics are a strong function of the initial electron profile, and the dose and energy of the proton implantation [5], [6]. While high temperature annealing is important for evaluating stability during high temperature processing, the main consideration for GaAs IC's is the long-term stability of the damaged layer at worst case operating temperatures. High temperature storage tests have been performed to evaluate the long-term reliability of proton isolation. The results are discussed in the next few paragraphs.

To accelerate the aging process, completed wafers were stored at 290°C and 350°C in nitrogen ambients. At numerous intervals during the stress tests, the wafers were removed from the furnaces, cooled to room temperature, and measured. The isolation voltage V_{iso} is measured on the test pattern in Fig. 7(a) and is defined as the voltage applied between the gate and ohmic contact with 1.0 μA of leakage current. The gate metallization is biased positively to determine the worst case isolation. In addition, the backgating threshold was measured on the test pattern

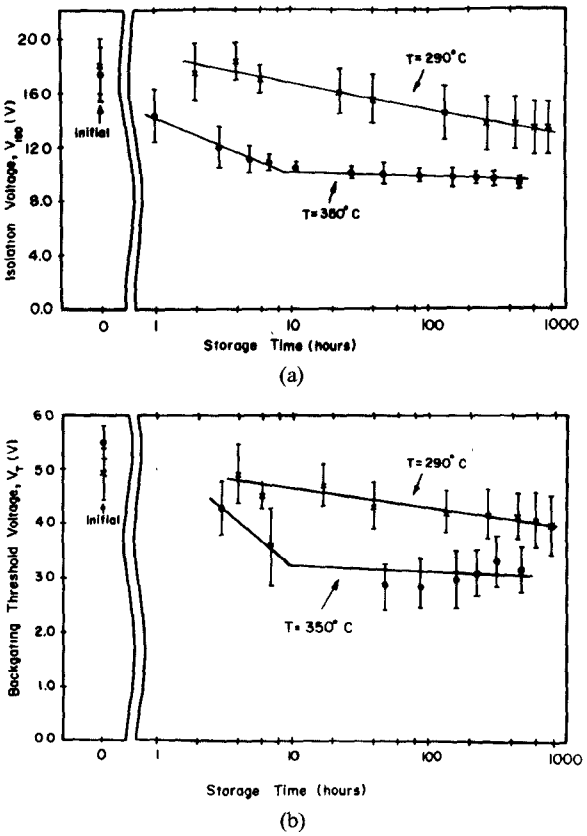

Fig. 13. Thermal stability of proton damage. (a) Isolation voltage V_{iso} versus storage time for two wafers, one stored at 290°C and the other stored at 350°C. The isolation voltage is measured at 1.0 μA on the test pattern diagrammed in Fig. 7(a). (b) Backgating threshold versus storage time for the two wafers included in (a). The backgating threshold is measured on the test pattern diagrammed in Fig. 9. The data points represent wafer averages (10 devices for V_{iso} and 35 devices for V_T) and the error bars indicate standard deviations.

diagrammed in Fig. 9. Both parameters are plotted as functions of high temperature storage time in Fig. 13(a) and (b). Two lightly Cr-doped wafers are included, one stored at 290°C and the other at 350°C. Each data point represents a wafer average, while the error bars indicate one standard deviation.

The results in Fig. 13(a) demonstrate a gradual logarithmic degradation in isolation voltage for the wafer stored at 290°C. Extrapolation of the data to longer storage times predicts a time to wafer-specification (8.5 V at 1.0 μA) exceeding 10^5 h. Similar behavior is observed for the backgating threshold voltage degradation at 290°C in Fig. 13(b). Again, a gradual logarithmic degradation rate dominates the aging characteristic with extrapolated failure times exceeding 10^5 h.

A more complex process is observed at 350°C. The isolation voltage in Fig. 13(a) decreases rapidly during the first 10 h of storage. However, the initial rapid degradation is then followed by an apparent saturation. The backgating threshold in Fig. 13(b) displays similar aging properties. The results imply that two or more annealing processes may be occurring simultaneously. A low activation energy process dominates at 290°C and during the initial stages at 350°C, while a second, higher activation energy process

dominates for long storage times at 350°C. These observations are consistent with recent identification of from three to five electron traps in proton implanted material [22]–[24].

The complex annealing behavior prevents the derivation of a single activation energy from the measured data. However, the extrapolated isolation and backgating threshold lifetimes of greater than 10^5 h at 290°C compare favorably with lifetimes between 10^3 and 10^4 h reported in the literature for commercial GaAs MESFET's aged at approximately 290°C [25], [26]. The high temperature storage tests imply that proton isolation is not the life time limiting component of the GaAs IC process. This conclusion is supported by measured results on a group of devices aged at an ambient temperature of 175°C. After 1500 h of storage, negligible changes in isolation voltages and backgating thresholds were observed.

IV. Summary

Proton implantation has been successfully employed in GaAs IC's to achieve dramatic improvements in isolation and backgating characteristics. In the IC, compatible process protons are implanted through the SiO_2 field oxide (the retained anneal cap) to simplify processing and to optimize surface passivation. An optimum proton dose and energy was determined from a systematic characterization of proton damage. The three-layer dielectric–Au mask is defined to 3-μm linewidths and is easily removed without damaging the exposed GaAs surface.

This process has achieved isolation voltages of 20 V between active regions separated by 3.0 μm, a factor of four improvement in comparison to a selective implant process. Backgating threshold voltages have been increased from −2.5 V for a selective implant process to −5.0 V for proton implantation on lightly Cr-doped substrates and −7.0 V for proton implantation on undoped substrates. These results indicate that proton isolation eliminates both isolation and backgating as design constraints.

High temperature storage tests have demonstrated that proton damage is thermally stable. Isolation lifetimes in excess of 10^5 h at 290°C have been observed. In addition, no measurable changes in isolation voltages or backgating thresholds were detected in devices stressed for 1500 h at 175°C. The high temperature storage tests imply that proton isolation does not limit the operating lifetime of a GaAs IC.

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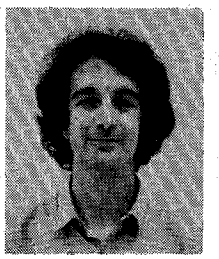

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Backgating in GaAs MESFET's

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Abstract—**The phenomenon of backgating in GaAs depletion mode MESFET devices is investigated. The origin of this effect is electron trapping on the Cr^{2+} and EL(2) levels at the semi-insulating substrate-channel region interface. A model describing backgating, based on DLTS and spectral measurements, is presented. Calculations based on this model predict that closely compensated substrate material will minimize backgating. Preliminary experimental data support this prediction.**

I. Introduction

THE characteristics of GaAs metal-semiconductor field effect transistors (MESFET's) depend strongly on the properties of the interface between the *n*-type active region and the semi-insulating substrate [1]. GaAs MESFET's can exhibit phenomena such as a drift in the drain current with time and a change in the drain current as a result of a change in the substrate bias. The decrease in the drain current when a negative voltage is applied to the substrate is termed backgating [2], [3]. Backgating is a detrimental effect in complex GaAs integrated circuits due to the interaction between closely spaced devices. This effect is caused by the relatively large capacitance of the substrate-active channel interface due to negative charge accumulated on deep traps in the interface region. The application of a bias to the substrate modulates this space charge region. This results in a change in the active channel region width and, therefore, a change in the drain current. In this paper, we will present the results of investigations into the physical nature of the deep traps responsible for backgating. Based on these investigations, we propose a model which explains backgating and demonstrate one solution, namely the use of closely compensated substrate material to minimize the back-side channel capacitance.

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II. Experimental Procedure

A. Substrate Material

GaAs MESFET's fabricated in four different types of substrate materials were investigated. The active region for the devices is produced by ion implantation into: 1) Cr-doped semi-insulating substrates (with Cr concentrations between 5×10^{15} and 1×10^{17} cm^{-3}); 2) high purity semi-insulating substrates (grown with no intentionally added dopants); 3) buffer layers on Cr-doped substrates; and 4) buffer layers on high purity substrates.

The substrate material, both Cr-doped and high purity, is grown by the two-atmosphere liquid encapsulated Czochralski (LEC) technique [4]. Chromium incorporates into the GaAs lattice on Ga sites and gives up three electrons to the bonds. The neutral state of Cr with respect to the lattice is Cr^{3+} with the electron configuration $3d^3$. Capture of electrons leads successively to the core states $3d^4$, Cr^{2+} (a singly, negatively charged acceptor), and $3d^5$, Cr^{1+} (a doubly, negatively charged acceptor). Chromium which is neutral, Cr^{3+}, is a double acceptor. The Cr^{2+} and Cr^{3+} levels are located 0.70 eV [5] and 0.45 eV [6] above the valence band, respectively, as shown in the energy level diagram of Fig. 1. There is uncertainty concerning the position of the Cr^{4+} and Cr^{1+} levels. According to the literature, the Cr^{4+} level is 0.15 eV [6] above the valence band and the Cr^{1+} level is degenerate with the conduction

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